

<b>Notice of References Cited</b>	Application/Control No. 09/772,920		Applicant(s)/Patent Under Reexamination CLEVENGER ET AL.	
	Examiner Belur V Keshavan		Art Unit 2825	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,529,953	06-1996	Shoda, Naohiro	438/644
*	B	US-6,284,642	09-2001	Liu et al.	438/622
*	C	US-6,165,898	12-2000	Jang et al.	438/638
*	D	US-6,313,003	11-2001	Chen, Sheng-Hsiung	438/396
*	E	US-6,319,813	11-2001	Givens, John H.	438/624
*	F	US-6,123,992	09-2000	Sugai, Kazumi	427/250
*	G	US-5,612,254	03-1997	Mu et al.	438/634
*	H	US-5,939,788	08-1999	McTeer, Allen	257/751
*	I	US-6,319,821	11-2001	Liu et al.	438/636
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	S. Wolf, Silicon Processing For The VLSI ERA-2, 1990, p194
	V	
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.